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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/468,015	12/20/1999	DIETMAR EGGERT	F71989US	3122

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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/468,015	EGGERT ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Amended Appeal Brief filed on December 14, 2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

KIM HUYNH
SUPERVISORY PATENT EXAMINER
3/2/03

Drawings

2. The drawings were received on May 10, 2002. These drawings are acceptable. However, the examiner requests that applicant resubmits pages 1-2 of the drawings - as a working set of the drawings with the examiner's notes (instead of the file copy) was inadvertently scanned. The scanned set will be used for publication.

Specification

3. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 2, 4, 5, 9, 11, 14, 15, 17, 18, 19, 20, 23 are objected to because of the following informalities:

"the group consisting of a substrate and an integrated circuit die" in line 3 of claim 2 should be replaced with "a group consisting of a substrate surface and an integrated circuit die surface" for proper antecedent basis and consistency

"a first and second end" in line 6 of claim 4 should be replaced with "a first end and a second end" for clarity

"second ends" in line 2 and "first ends" in line 3 of claim 5 should be replaced with "second end" and "first end" respectively - as each coil turn only has one first end and one second end

"is" in line 1 of claim 9 should be replaced with "are"

"is" in line 2 of claim 11 should be replaced with "are"

"ESD claim" in line 1 of claim 14 should be replaced with "ESD clamp"

"a one of said plurality of ESD claim devices" in line 2 of claim 15 should be replaced with "one of said plurality of ESD clamp devices"

"ESD claim" in line 1 of claim 17 should be replaced with "ESD clamp"

"such that such that" in line 6 of claim 18 should be replaced with "such that"

"the step of" in lines 1, 2 of claim 19 should be deleted as it depends on a claim that does not recite step(s)

"device", in the first instance in line 2 of claim 19 should be replaced with "devices"

"the step of" in lines 1, 2 of claim 20 should be deleted as it depends on a claim that does not recite step(s)

"a one" in line 3 of claim 20 should be replaced with "one"

"the group consisting of a substrate and an integrated circuit die" in line 3 of claim 23 should be replaced with "a group consisting of a substrate surface and an integrated circuit die surface" for proper antecedent basis and consistency.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

Claim 1 recites the limitation "said plurality of ESD clamp devices being connected to a corresponding one of said plurality of turns of said inductor" in lines 6-8. Claim 1 is indefinite because it is not clear whether all the ESD clamp devices are connected to one turn of the inductor, each ESD clamp device is connected to one corresponding turn of the inductor, two or more ESD clamp devices of the plurality of ESD clamp devices are connected to each turn of the inductor, or at least one ESD clamp device is connected to a two or more turns of the inductor. It is further not clear what the term "corresponding" means in the context of the claim.

Claim 4 recites in lines 15-17 a limitation similar to the limitation in claim 1, and is indefinite for the same reasons.

Claim 6 recites in lines 1-2 the limitation "each of the respective ones of said plurality of conductive vias is at least one via". It is not clear how each via is at least one via, (e.g. how each via is two vias). It appears that applicant meant for the two adjacent conductive layers of the plurality of conductive layers to be connected by at least one via.

Claim 7 recites in lines 1-2 the limitation "each of the respective ones of said plurality of conductive vias is two or more vias". It is not clear how each via is two or more vias. It appears that applicant meant for the two adjacent conductive layers of the plurality of conductive layers to be connected by two or more vias.

Claim 11 recites the limitation "said plurality of conductive layers" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites in lines 14-15 a limitation similar to the limitation in claim 1, and is indefinite for the same reasons.

Claim 21 recites in lines 6-8 a limitation similar to the limitation in claim 1, and is indefinite for the same reasons.

The rejections that follow are made based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (US 5,969,929).

Kleveland teaches an ESD protection network [FIG. 2A; FIG. 7], comprising:

an inductor [e.g. 720, FIG. 7] having a plurality of turns in the shape of a coil, the plurality of turns having an inductance [col. 7, lines 27-35]; and

a plurality of ESD clamp devices [718, 719 - FIG. 7], each one of said ESD clamp devices having a parasitic capacitance [col. 1, lines 35-38], one ESD clamp device being connected to a corresponding one of said plurality of turns of said inductor [center of the spiral 720 connected to ESD 718: col. 7, lines 35-38], the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter [FIG. 2A shows a plurality of inductors and the plurality of ESD devices forming a low pass filter structure - see definition and illustration of low pass filter on page 413 of "The Illustrated Dictionary of Electronics"].

Kleveland, therefore, discloses the invention except for a plurality of ESD clamp devices being connected to an inductor. Since it was known in the art at the time the invention was made to use additional ESD clamp devices to provide additional ESD protection, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a plurality ESD clamp devices (instead of a single ESD clamp device) for connection with the inductor, in order to provide additional ESD protection.

Kleveland further teaches the inductors and the plurality of ESD clamp devices being fabricated on a substrate and an integrated circuit die.

10. Claims 4-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Kleveland in view of Ling (US 5,576,680).

11. As per claims 4-13, 15-18, 20-24, Kleveland discloses the ESD network above, but does not disclose each of the turn of one inductor being formed on a separate layer of the integrated circuit. Kleveland, however, teaches using conventional CMOS processes to fabricate the ESD circuit [col. 7, lines 38-42].

Ling discloses several processes of fabricating inductive circuit on an IC in a non-planar configuration [FIG. 4A shows a process for forming the inductive circuit 400 by connecting a plurality of turns [410-430] formed on different horizontal planes of the IC connected by vias [440-1, 440-2: col. 8, lines 8-20] to better reflect the continuous spiral shape and property of an inductor [col. 1, lines 18-51]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the non-planar configuration aspect of an inductor, as is taught by Ling, in fabricating the inductors of Kleveland in order to better reflect the continuous spiral shape and property of an inductor.

Ling further discloses via 440-1 connecting the second end of coil turn 410 to the first end of coil turn 420, and via 440-2 connecting the second end of coil turn 420 to the first end of coil turn 430 [FIG. 4A]; furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use two or more vias to connect the coil turn since it was known in the art to use more than one vias for connection to reduce electrical connection resistance.

Ling also teaches the shape of the coil turns being rectangle or square [FIG. 4A].

Kleveland teaches the inductor being made of metal [col. 7, line s27-35], but

does not disclose the type of material. Since applicant has not disclosed that the type of material solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with any metal known to be used in the art for conductivity [page 11, lines 4-7], it would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper for example to implement conductivity in the inductor. A similar argument is made with respect to the inductor being made of conductive doped polysilicon.

Ling also teaches a magnetic inductive core [Abstract, lines 4-6] interposed concentrically inside of an inner diameter of the coil turns [125-1, FIG. 1E], but does not disclose the type of magnetic material. Since applicant has not disclosed that the type of material solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with any metal known to be used in the art for a magnetic inductive core [page 11, lines 4-7], it would have been obvious to one of ordinary skill in the art at the time the invention was made to use iron for example as the magnetic material for the magnetic inductive core.

Kleveland further teaches the coil turn in the central of the spiral being connected to an ESD device; the ESD devices being fabricated on the IC substrate and connected to the inductor with vias [235-236, FIG. 2B]; Ling teaches the vias through the plurality of insulation layers [FIG. 4A].

12. As per claims 14, 19, Kleveland teaches an ESD protection network [FIG. 2A; FIG. 7], comprising:

an inductor having a plurality of turns [a plurality of impedance components 214-

217, FIG. 2A, each component having a plurality of turns, the inductor having the combined turns of all the impedance components] in the shape of a coil [720-721, Fig. 7], the plurality of turns having an inductance [col. 7, lines 27-35]; and

a plurality of ESD clamp devices [220-223, FIG. 2A; 718-719, FIG. 7], each one of said ESD clamp devices having a parasitic capacitance [col. 1, lines 35-38], at least one ESD clamp device being connected to a corresponding one of said plurality of turns of said inductor [720 connected to ESD 718, 721 connected to ESD 719: col. 7, lines 35-38; see also FIG. 2A], the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter [FIG. 2A shows a plurality of inductors and the plurality of ESD devices forming a low pass filter structure - see definition and illustration of low pass filter on page 413 of "The Illustrated Dictionary of Electronics"].

Kleveland does not disclose each of the turn of an inductor being formed on a separate layer of the integrated circuit. Kleveland, however, teaches using conventional CMOS processes to fabricate the ESD circuit [col. 7, lines 38-42].

Ling discloses several processes of fabricating inductive circuit on an IC in a non-planar configuration [FIG. 4A shows a process for forming the inductive circuit 400 by connecting a plurality of turns [410-430] formed on different horizontal planes of the IC connected by vias [440-1, 440-2: col. 8, lines 8-20] to better reflect the continuous spiral shape and property of an inductor [col. 1, lines 18-51]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the non-planar configuration aspect of an inductor, as is taught by Ling, in fabricating the

inductors of Kleveland in order to better reflect the continuous spiral shape and property of an inductor.

The combination above does not teach at least one ESD clamp device being connected to each one of said plurality of conductive layers (i.e. at least one ESD clamp device connected to each coil turn). Essentially, the combination above does not teach the impedance components being single-turn. Since it was known in the art at the time the invention was made to alternatively use a multiple turn impedance component with a smaller width line, or a single turn impedance component with a wider width line, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use single turn impedance components with wider width line as an alternative to using single turn impedance components with smaller width line, in order to implement conductivity in the inductor.

Response to Arguments

13. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

14. For the record, the examiner submits that the claims in CLAIMS APPENDIX (section VIII) of the Appeal Brief filed December 14, 2005 reflect the correct pending claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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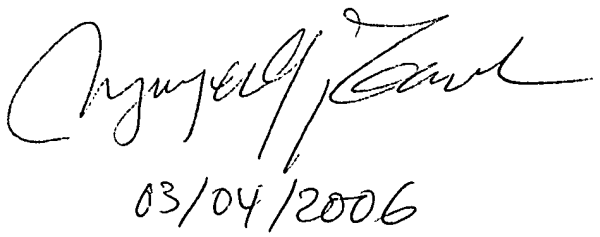

03/04/2006

TQN

March 4, 2006